EVEN NUCLEATION BETWEEN SILICON AND OXIDE SURFACES FOR THIN SILICON NITRIDE FILM GROWTH

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application a division of U.S. Patent Application Serial No. 10/139,987 filed May 7, 2002, now Patent No. 6,787,834 which is a division of U.S. Patent Application Serial No. 09/975,879 filed October 12, 2001, now U.S. Pat. No. 6,498,063.

BACKGROUND OF THE INVENTION

[0002] The present invention pertains to semiconductor fabrication processing and more particularly to a method for providing even nucleation between silicon and oxide surfaces for uniformly thin silicon nitride film growth used in semiconductor devices, such as dynamic random access memories (DRAMs).

[0003] In the manufacturing of dynamic random access memories (DRAMs), the size of the memory cell is the main contributing factor to the density and overall size of the device. A manufacturer of DRAMs has motivation to increase the storage capability, while maintaining the smallest die size possible, as the smaller die size results in a lower cost per device. As mentioned, the main contributor to the size of a memory device is the amount of space required for each storage cell that makes up the storage array. In that regard, DRAM fabrication engineers have focused on structures, on materials to make the structures and on methods to fabricate the structures necessary to make a storage cell.

[0004] To save space, the capacitor of the storage cell must reduce in size and yet maintain adequate capacitance to retain a sufficient charge during DRAM operation. There are several approaches to the capacitor design, for example trench capacitors formed in the substrate of a wafer or a stacked capacitor formed above the wafer substrate, to name two. Regardless of the design chosen, the size of the capacitor must be reduced and yet maintain sufficient capacitance as mentioned previously. Two of the main contributors to capacitance are the surface area of the